



INNOVATION

ANYTHING-ON-ANYTHING

BIG IDEA CONFERENCE | SEPTEMBER 20th, 2022



DISCLAIMER

This document is provided by Soitec (the “Company”) for information purposes only.

The Company’s business operations and financial position are described in the Company’s 2021-2022 Universal Registration Document (which notably includes the 2021-2022 Annual Financial Report) which was filed on June 20th, 2022, with the French stock market authority (Autorité des Marchés Financiers, or AMF) under number D.22-0523 as well as in the Company’s FY’22 half-year report released on December 2nd, 2021. The French versions of the 2021-2022 Universal Registration Document and of the half-year report, together with English courtesy translations for information purposes of both documents are available for consultation on the Company’s website (www.soitec.com), in the section Company - Investors - Financial Reports.

Your attention is drawn to the risk factors described in Chapter 2.1 of the Company’s 2021-2022 Universal Registration Document.

This document contains summary information and should be read in conjunction with the 2021-2022 Universal Registration Document.

This document contains certain forward-looking statements. These forward-looking statements relate to the Company’s future prospects, developments and strategy and are based on analyses of earnings forecasts and estimates of amounts not yet determinable. By their nature, forward-looking statements are subject to a variety of risks and uncertainties as they relate to future events and are dependent on circumstances that may or may not materialize in the future. Forward-looking statements are not a guarantee of the Company’s future performance. The occurrence of any of the risks described in Chapter 2.1 of the Universal Registration Document may have an impact on these forward-looking statements. In addition, the future consequences of geopolitical conflicts, in particular the Ukraine / Russia situation, as well as rising inflation, may result in greater impacts than currently anticipated in these forward-looking statements.

The Company’s actual financial position, results and cash flows, as well as the trends in the sector in which the Company operates may differ materially from those contained in this document. Furthermore, even if the Company’s financial position, results, cash-flows and the developments in the sector in which the Company operates were to conform to the forward-looking statements contained in this document, such elements cannot be construed as a reliable indication of the Company’s future results or developments.

The Company does not undertake any obligation to update or make any correction to any forward-looking statement in order to reflect an event or circumstance that may occur after the date of this document. In addition, the occurrence of any of the risks described in Chapter 2.1 of the Universal Registration Document may have an impact on these forward-looking statements.

This document does not constitute or form part of an offer or a solicitation to purchase, subscribe for, or sell the Company’s securities in any country whatsoever. This document, or any part thereof, shall not form the basis of, or be relied upon in connection with, any contract, commitment or investment decision.

Notably, this document does not constitute an offer or solicitation to purchase, subscribe for or to sell securities in the United States. Securities may not be offered or sold in the United States absent registration or an exemption from the registration under the U.S. Securities Act of 1933, as amended (the “Securities Act”). The Company’s shares have not been and will not be registered under the Securities Act. Neither the Company nor any other person intends to conduct a public offering of the Company’s securities in the United States.

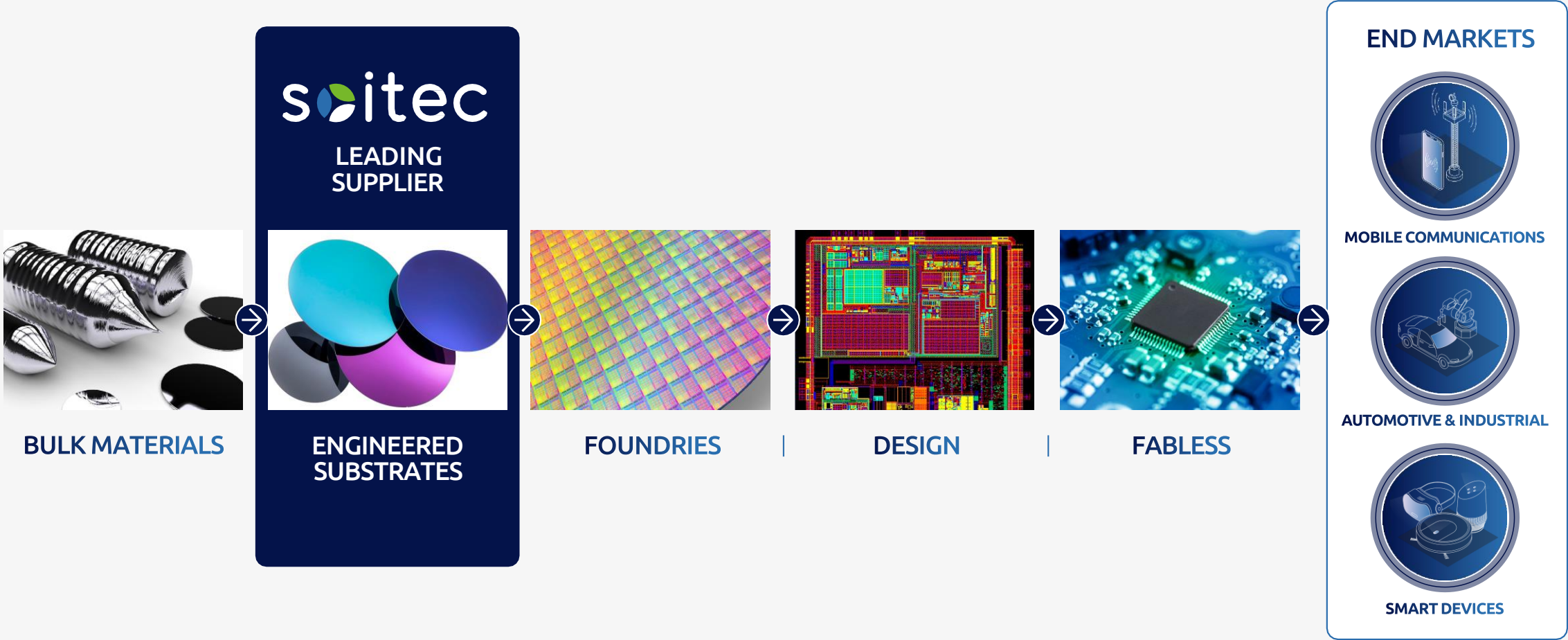
SECTION 01

INTRODUCTION TO SOITEC



SOITEC HAS BUILT A UNIQUE POSITION IN THE SEMICONDUCTOR INDUSTRY

LEVERAGING STRATEGIC PARTNERSHIPS IN THE ENTIRE SEMICONDUCTOR ECOSYSTEM



WE HAVE DEVELOPED A COMPREHENSIVE PRODUCT PORTFOLIO

FOCUSING ON OUR 3 STRATEGIC END MARKETS

MOBILE COMMUNICATIONS



MAIN DRIVERS

- 5G Sub-6 GHz
- 5G mmWave
- Mobile infrastructure & SatCom
- Wi-Fi 6, 6E & 7

SOITEC PRODUCTS

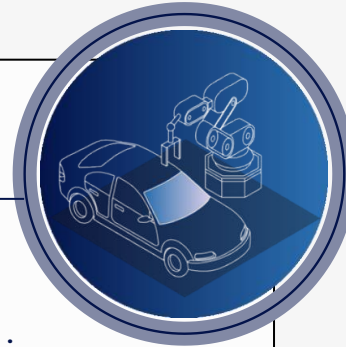
Connect RF-SOI

Connect FD-SOI

Connect POI

Connect RF-GaN

AUTOMOTIVE & INDUSTRIAL



MAIN DRIVERS

- Autonomous cars
- Vehicle electrification
- Infotainment
- Industry 4.0

SOITEC PRODUCTS

Auto Power-SOI

Auto FD-SOI

Auto SmartSiC™

Auto Power-GaN

SMART DEVICES



MAIN DRIVERS

- Edge computing
- 3D sensing & Healthcare
- Smart home & Smart cities
- Data centers

SOITEC PRODUCTS

Smart FD-SOI

Smart Imager-SOI

Smart Photonics-SOI

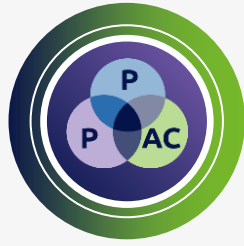
Smart PD-SOI

SECTION 02

SOITEC INNOVATION STRATEGY



KEY CONTRIBUTORS TO ENABLE GROWTH



PPAC



TIME TO MARKET



SUSTAINABILITY



Continue Moore's Law

New architectures

New structures / 3D

New materials

New ways to shrink

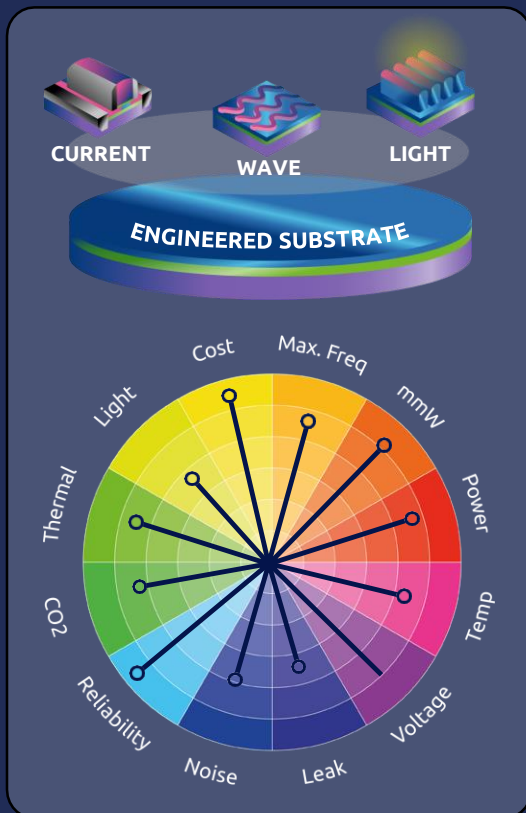
Advanced packaging



soitec

ENGINEERED
SUBSTRATES

ENGINEERED SUBSTRATES CREATE VALUE AT THE SYSTEM LEVEL



Combining physical
properties of materials



CONNECT

Data rate, power efficiency



COMPUTE

Energy efficiency performance,
data rate with photonics



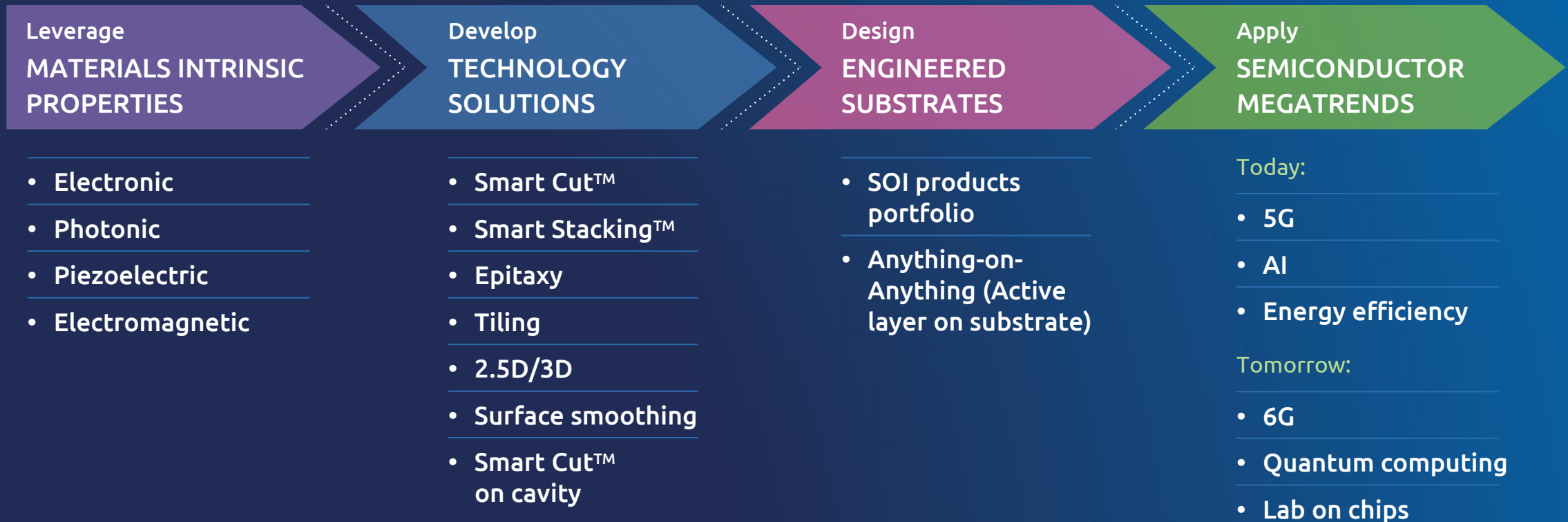
SENSE

3D imaging, health sensors

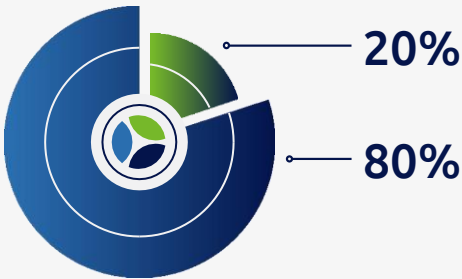
POWER

Power density, higher efficiency

LEVERAGING MATERIALS SCIENCE TO ENABLE UNIQUE APPLICATIONS



BALANCING SHORT-TERM INNOVATION AND FUTURE OPPORTUNITIES



2022

2026

2030

PRODUCTS UNDER DEVELOPMENT TO SUPPORT OUR BP

TECHNOLOGIES AND PRODUCTS INCUBATION

Addressing short and medium-term differentiations for our customers

INCREMENTAL INNOVATION

SOI next generation

POI next generation

SOI for MEMS

SmartSiC™

To support future opportunities and growth

DISRUPTIVE INNOVATION

Tiling for large diameters

2.5D/3D

InP - photonics, 6G

Materials science

Compound integration

SUBSTRATE INNOVATION CENTER

UNIQUE CAPABILITIES FOR INNOVATIVE SUBSTRATE TECHNOLOGIES



INFRASTRUCTURE

- World class material characterization lab and metrology
- Large choice of equipment/toolset
- Comprehensive material science & engineering
- On-site dedicated engineers from Soitec

PROGRAMS

- SmartSiC™
- New generation FD-SOI and RF-SOI
- 300mm InP on Si
- Low temperature Smart Cut™ for 3D integration
- ...

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Pilot Line at CEA-Leti for early prototyping of new substrate technologies
(focus on lead time and quality)

SECTION 03

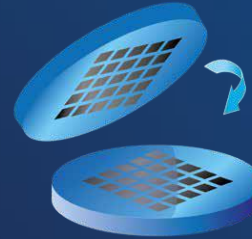
SOITEC INNOVATION TOOLBOX



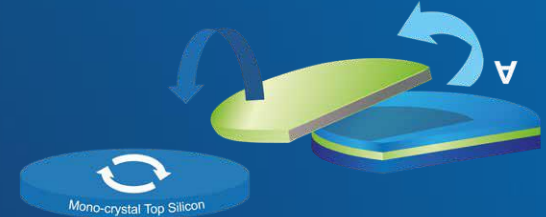
SOITEC CORE TECHNOLOGY TOOLBOX



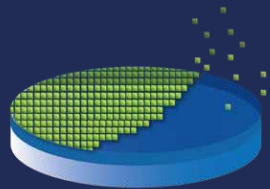
Smart Cut™



Smart Stacking™



Refresh - Repolish



Epitaxy

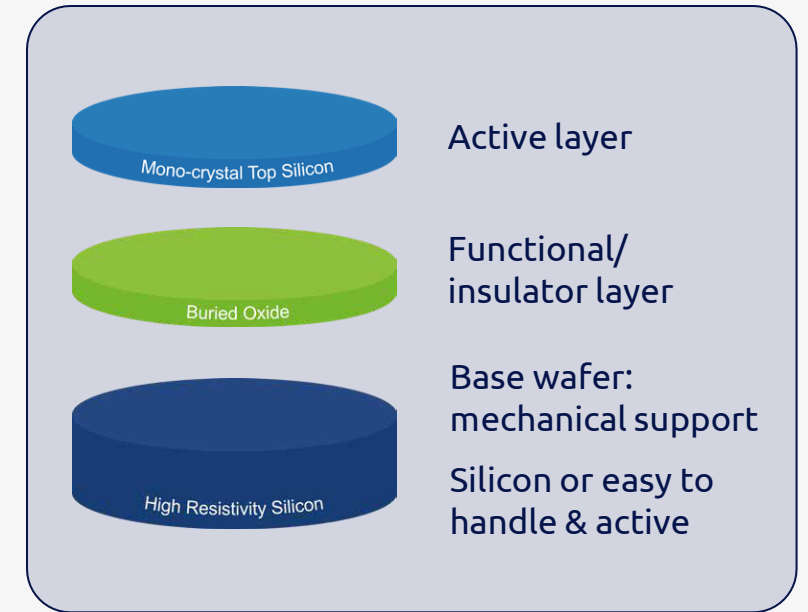
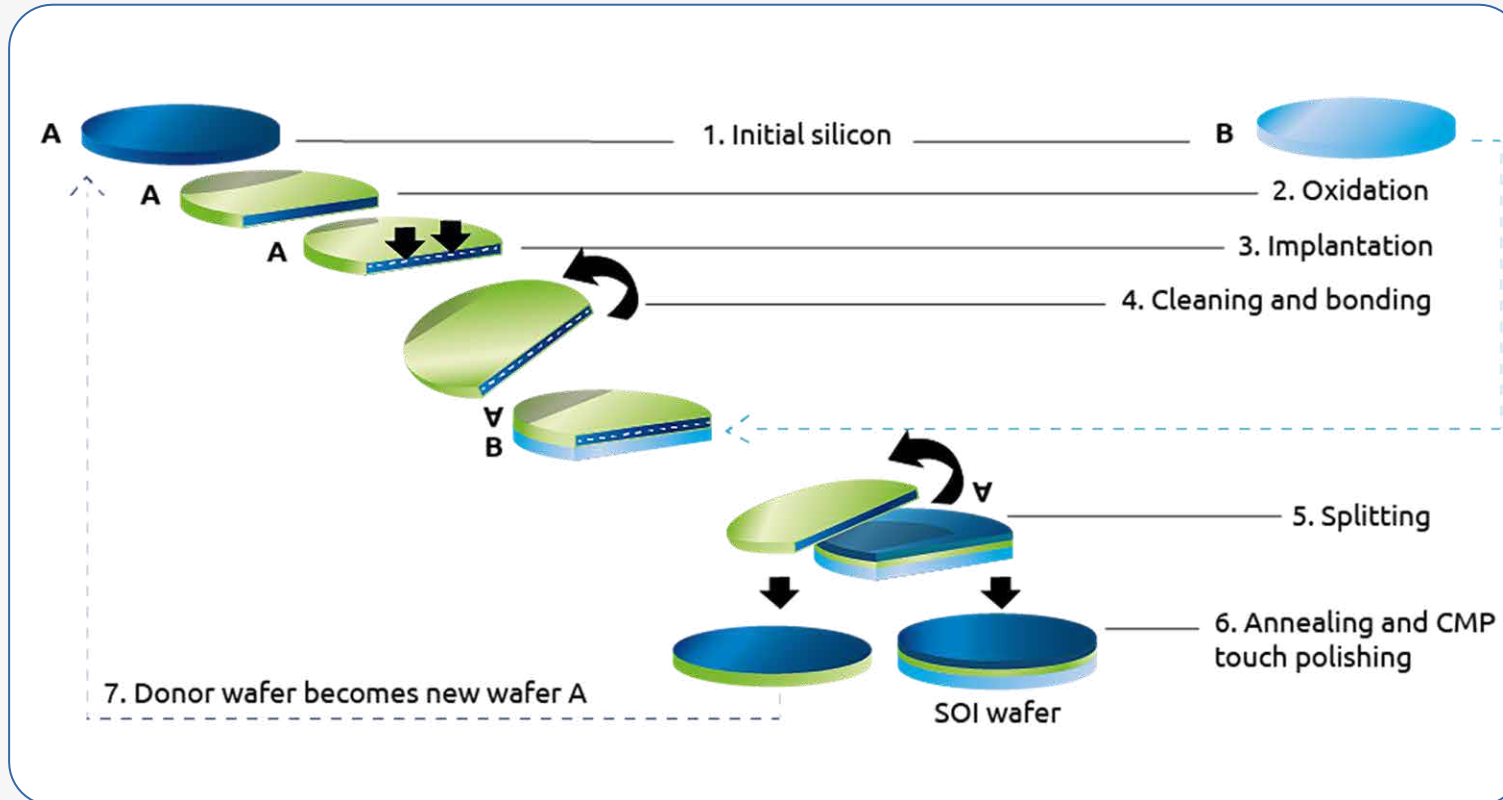


Material Expertise



Advanced Processing

SMART CUT™ AND SOI SUBSTRATES

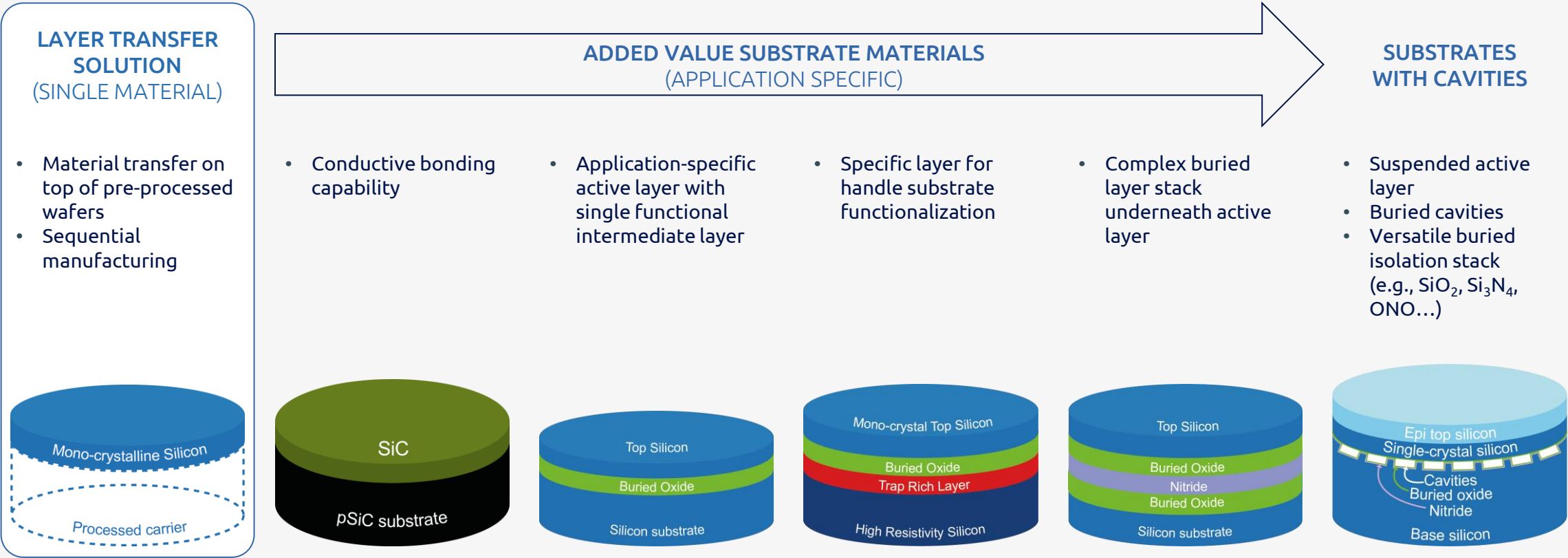


TECHNOLOGY

- Industrial manufacturability of SOI – high yield
- Drastic improvement in uniformity & quality
- Re-use of donor wafer increases cost efficiency
- Flexibility of material integration


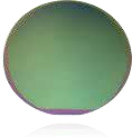







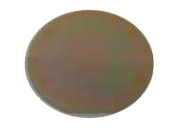






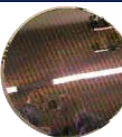

VERSATILE SUBSTRATES TECHNOLOGY

OFFERING OUR CUSTOMERS **SUBSTRATE DESIGN** FOR **PERFORMANCE, ENERGY EFFICIENCY, INTEGRATION AND COST BENEFITS** THANKS TO A WIDE RANGE OF OPTIONS TO ENGINEER SUBSTRATES



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BEST ACTIVE LAYER(S) ON FUNCTIONAL SUBSTRATE

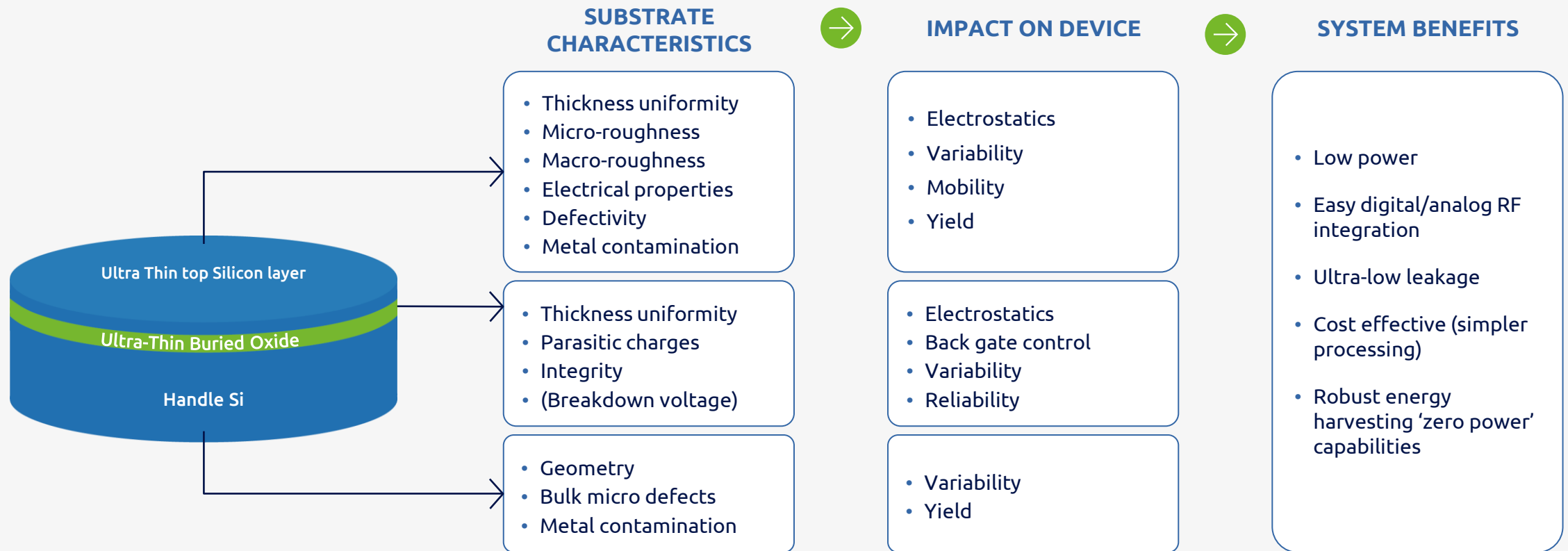
		ACTIVE LAYER						
		Silicon	Piezo	SiC	InP	GaN	GaAs	Ge
SUBSTRATE	Silicon							
	Sapphire							
	SiC							
	GaAs							
	Device wafer							

ANYTHING-ON-ANYTHING

BEST ACTIVE LAYER(S) ON FUNCTIONAL SUBSTRATE

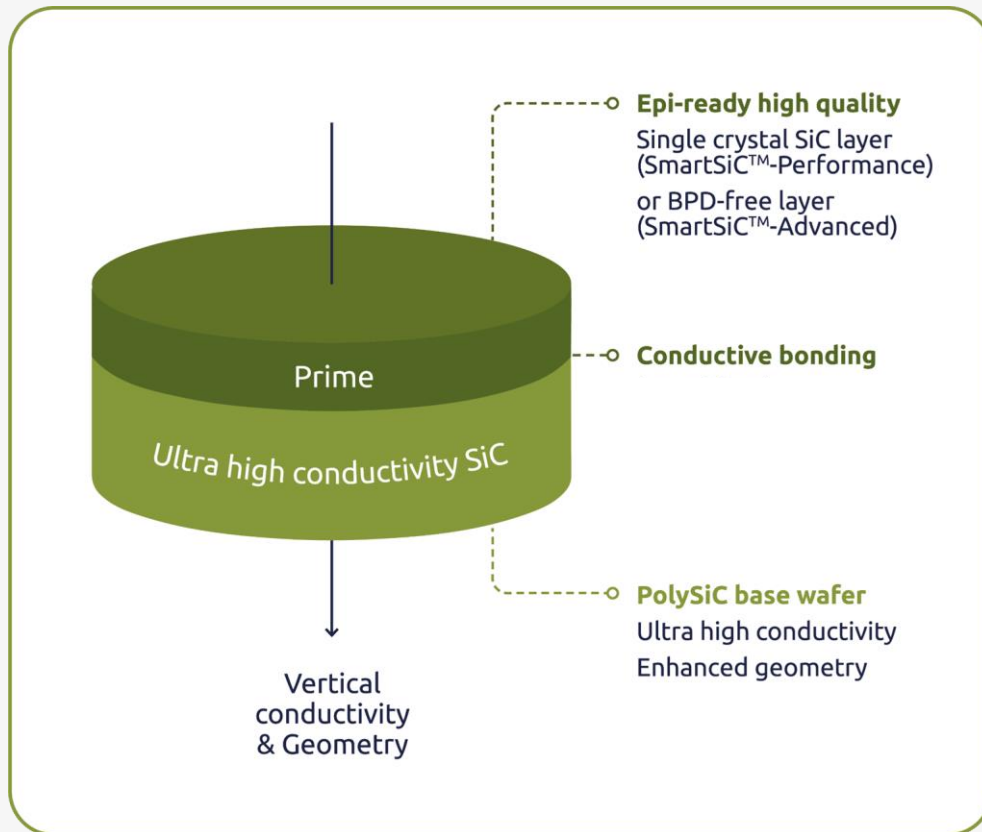
		ACTIVE LAYER						
		Silicon	Piezo	SiC	InP	GaN	GaAs	Ge
SUBSTRATE	Silicon	Low power Transistor isolation Radiation hardness Edge AI, 4G/5G, Data Center, Imager	High performance RF filters 4G/5G	Co-integration Quantum	Co-integration Scalable to 300mm High performance 6G, SWIR, Imager	PA performance Co-integration 5G/6G, smartphones	Co-integration Scalable to 300mm Optoelectronics	Co-integration Scalable to 300mm High mobility Optoelectronics
	Sapphire	Transistor isolation Radiation hardness 3G/4G			Co-integration High performance Optoelectronics	High performance microLEDs	Co-integration High performance Optoelectronics	Co-integration High performance Optoelectronics
	SiC			Better performance Higher yield Green technologies Power electronics		PA performance Co-integration 5G/6G, baseband		
	GaAs				Optical performance Optoelectronics		Optical performance Optoelectronics	
	Device wafer	Uniformity Crystal quality SoC integration 3D Sequential integration	Uniformity Crystal quality yield Sensors, Actuators					

FD-SOI – BRINGING AI ONTO THE EDGE WITH LOW ENERGY CONSUMPTION



ANYTHING-ON-ANYTHING APPLICATIONS

SMARTSiC™ – BONDING 2 DIFFERENT SUBSTRATES ALLOWS FOR LOWER RESISTIVITY WITH CONSTANT DEFECTIVITY



VALUE PROPOSITION

SmartSiC™ vs. SiC: **Greener, Faster and Better**

- 20,000 Tons of CO₂ reduction for each 500,000 wafers vs. SiC
- 200mm scalability to accelerate SiC adoption through 10x re-usability
- Enabling new generations of SiC devices thanks to an improvement of resistivity of up to 30%
- Reducing Capex & Opex for device manufacturers

ANYTHING ON ANYTHING AS A PERFORMANCE CATALYST

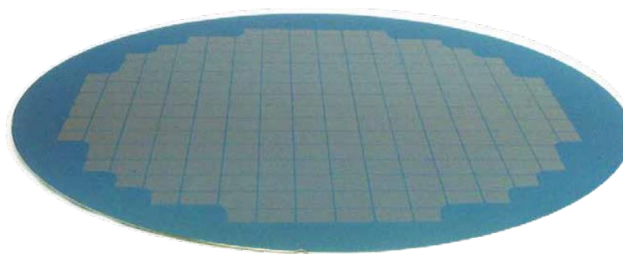
- Significant improvement of resistivity through doping while maintaining low defectivity
- Prime layer of single-crystal SiC, with very low doping and high quality crystal, has a minimal contribution to vertical conductivity given thinness
- Thicker Ultrahigh-conductivity SiC (polySiC) layer can be properly doped without affecting crystal quality

ANYTHING-ON-ANYTHING APPLICATIONS

TILING - EXAMPLE WITH InP



InP bulk
100mm



InP on Silicon
200mm

ENABLING InP FOR SEVERAL APPLICATIONS

- High frequency devices (RF, THz, 5G/6G, ...)
- Optoelectronics & Photonics (lasers, 3D sensing, PICs, gas sensing, ...)
- SWIR Image sensors
- Energy harvesting (IR, solar cells, ...)

InP SUBSTRATE TECHNOLOGIES FOR RF APPLICATIONS

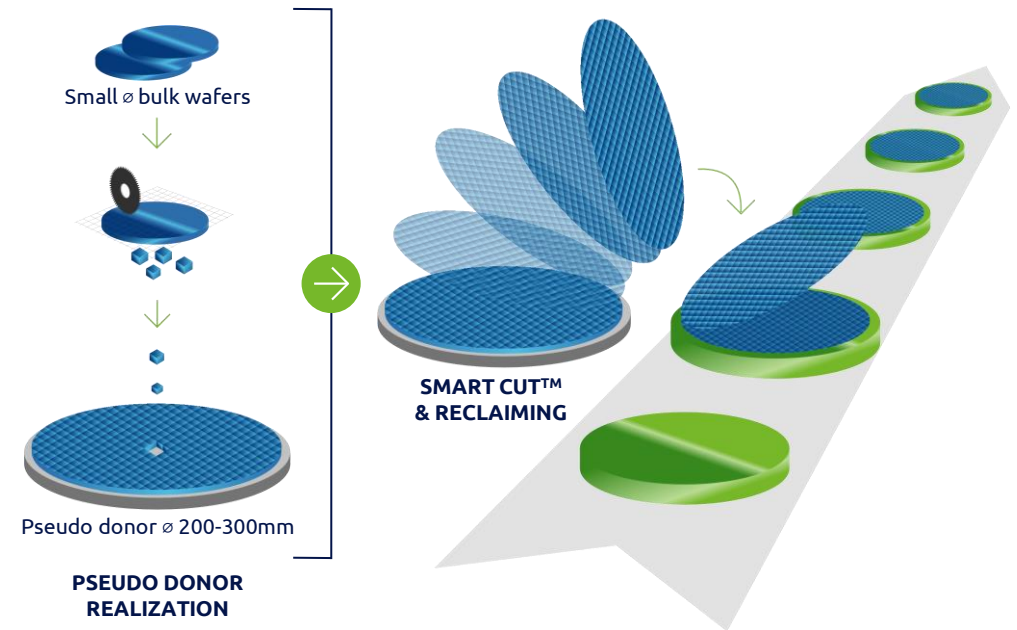
Smart Cut™ “InP-on-Anything”

- Handle substrate: Silicon, GaAs,...
- Donor substrate reclaiming
- but limited to 4-6 in diameter



Tiling for InP

- Scaling to larger wafer diameter (up to 12in)
- Handle substrate: Silicon (bulk or device wafer)
- Versatile die size and geometries



ANYTHING-ON-ANYTHING APPLICATIONS

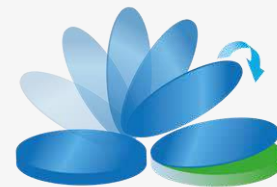
TOWARDS HIGH DENSITY 3D DEVICE STACKING

3D Integration benefits

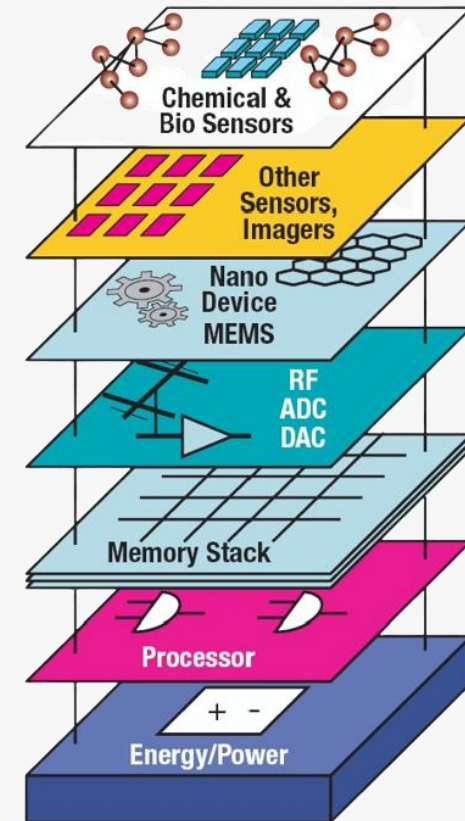
- Higher performance and density
- Higher functionality
- Smaller form factor
- Cost reduction

3D Monolithic adds further value

- Front end device integration
- Very dense device integration by nm alignment



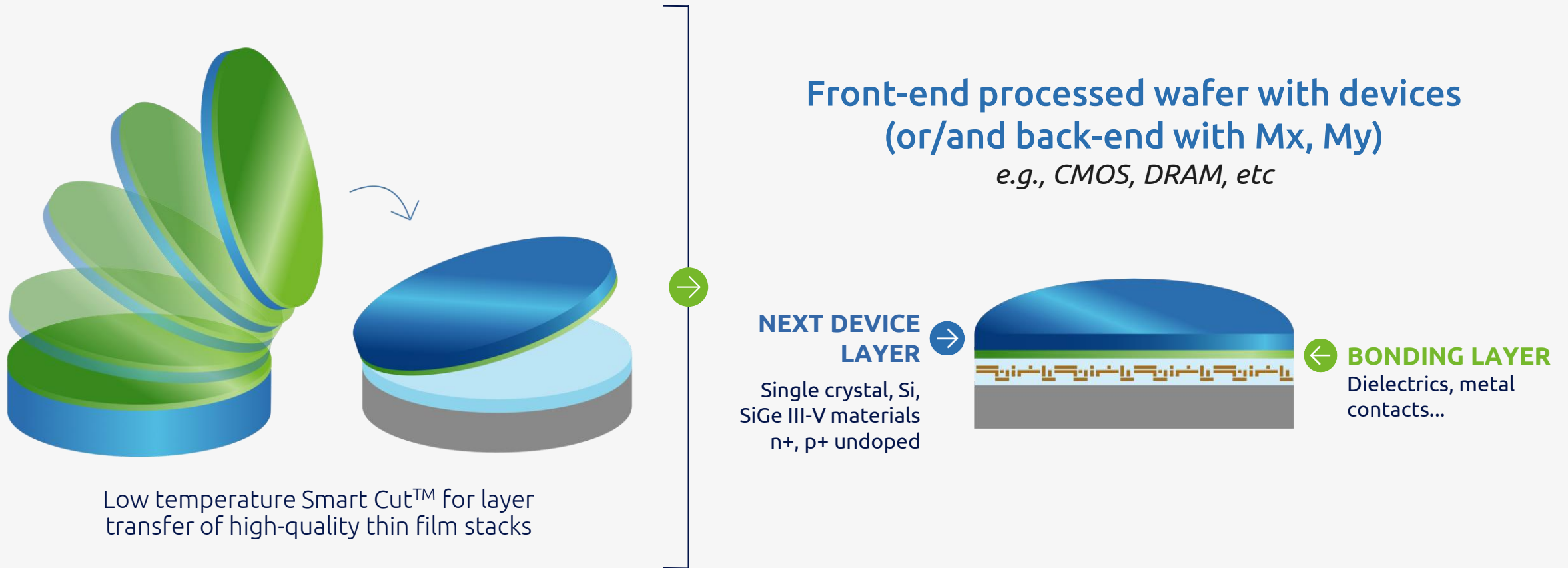
Smart Cut™



Courtesy of Pr. James J.-Q. Lu, IEEE fellow
A New Paradigm for Future Technologies

ANYTHING-ON-ANYTHING APPLICATIONS

3D LAYER STACKING BY SMART CUT™



INNOVATION TAKEAWAYS

INNOVATION AT THE HEART OF SOITEC SUSTAINABLE VALUE CREATION MODEL

- We are transforming our Innovation to meet short to long-term market needs
- Our Innovation is enabling 20-25% annual growth towards ~2.3bn revenue in FY26

ENGINEERED SUBSTRATES AND SEMICONDUCTOR INNOVATION

- Leveraging materials science through engineered substrates
- PPACT is driving our innovation strategy
- SmartSiC™ technology demonstrated, actively working on prototyping and qualifying with several customers

SOITEC INNOVATION MODEL

- Maturing & sharpening our technologies to bring best layer on best substrate
- Strengthening our collaboration model
- Developing products fitted for High Volume Manufacturing



THANK YOU

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